ABSTRACT

Cache coherency rules for a multi-processor computing system that is capable of working with compressed cache lines' worth of information are described. A multi-processor computing system that is capable of working with compressed cache lines' worth of information is also described. The multi-processor computing system includes a plurality of hubs for communicating with various computing system components and for compressing/decompressing cache lines' worth of information. A processor that is capable of labeling cache lines' worth of information in accordance with the cache coherency rules is described. A processor that includes a hub as described above is also described.